A2

8. The method of claim 1 wherein the non-native instructions are variable length X86 instructions.

A3

10. An apparatus for processing program instructions comprising:

a buffer coupled to receive at least one instruction containing data representing operational code and data representing at least one flag modification enable bit;

a variable length instruction emulator that uses fixed length native instructions as the at least one instruction, to emulate variable length instructions wherein the variable length instruction emulator emulates non-native instructions using native instructions containing the flag modification enable bit; and

a controller operatively responsive to the at least one instruction stored in the buffer, that determines whether the at least one flag modification enable bit allows updating of at least one flag in response to executing the operational code and that updates at least one flag in response to determining a status of the at least one flag modification enable bit.

A4

17. The apparatus of claim 10 wherein the non-native instructions are variable length X86 instructions.